Performance metrics estimation in IC process flow by using TCAD simulations

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Abstract:

The IC fabrication flow has many process steps, which should be well chosen for an optimized performance. In our study few process steps have been investigated for improving the performance by using the process simulation of Synopsys TCAD. This work includes processes such as oxidation, diffusion and annealing mechanisms. An optimized result for oxidation is presented by considering the different temperature conditions at different time slots. An important mechanism such as channelling is well estimated and proved an angle of 7^{o} is the sophisticated value for reducing the channelling mechanism. And finally annealing mechanism has been investigated and the results were reported.

Key words: *IC, oxidation, diffusion, channelling, annealing, TCAD.*

Resumen:

El flujo de fabricación de IC tiene muchos pasos de proceso, que deberían ser bien elegidos para un rendimiento optimizado. En nuestro estudio, se han investigado algunos pasos del proceso para mejorar el rendimiento mediante el uso de la simulación de proceso de Synopsys TCAD. Este trabajo incluye procesos tales como mecanismos de oxidación, difusión y recocido. Se presenta un resultado optimizado para la oxidación considerando las diferentes condiciones de temperatura en diferentes intervalos de tiempo. Un mecanismo importante como la canalización está bien estimado y se ha demostrado que un ángulo de 7o es el valor sofisticado para reducir el mecanismo de canalización. Y finalmente se ha investigado el mecanismo de recocido y se informaron los resultados.

Palabras clave: IC, oxidación, difusión, canalización, recocido, TCAD.

I.Introduction

TCAD is the process and device design tool in the device manufacturing environment. It can able to combine the bridge gap between IC design and manufacturing. The most important factor of this tool is to reduce the yield and fluctuation losses occur in manufacturing technology and providing the guidelines for optimizing the device before manufacturing [Bork et. al, C.D. Krzeminski et. al].

The processing steps are the major techniques in IC fabrication. There is an abundant literature available for performing these processes in a sophisticated method in order to fabricate required device structure [W. Jungling et. al] . Oxidation, diffusion and Lithography are one of the most important process steps in the fabrication technology.

The mechanisms used for oxidation and its growth rate for different time slots and its variations with respect to the temperature conditions. The important techniques that should be used for growing a quality of oxide, higher growth rate and various oxide materials are well defined. In particularly the thermal oxidation which is mainly used for the devices like Metal oxide Semiconductor Field Effect Transistor is well explained. As per the literature various works under this mechanism have been reported. Steam oxidation on silicon [L.E. Katz et. al], high pressure oxidation on Si [H. Miyoshi et.al, L.N. Lie et. al] and its kinetics [R.R. Razouk et. al], multi-layer growth of oxide [D. Fang et. al], oxide based thin films [H.S. Oon et. al], synthesis of iron oxide [R. Baca et. al] and various techniques for internal oxidation have been reported [X. Xu et. al]. Many dielectric materials have been reported for the gate-oxide replacement such as SiO_2, Si_3N_4, HfO_2, ZrO_2, Al_2O_3, La_2O_3, TiO_2, Ta_2O_5, and Y_2O_3. Recently, an alternative material has been reported for the replacement of oxide as the gate-oxide material such as lanthanide (called as rare earth oxide) [K.H. Goh et. al].

Even though many diffusion techniques are available, the recent diffusion process like ion-implantation techniques and its features has been stated as the well-organized fabrication techniques [H. Miyoshi et.al]. Several methods to determine the range in this diffusion process have been reported [K. Nordlund et. al, D. Cai et. al]. As the implantation technique has much flexibility in order to penetrate the ions in the crystals with various direction alignments of the crystals [O.S. Oen et. al, L.T. Chadderton et. al, J.F. Ziegler et. al, J. Sillanpää et. al]. In order to heal the defects caused by this diffusion, a process called as Annealing is studied with different temperature conditions and the outcomes are reported. Many works have been carried out related to the Lithography process. diffusion enhancement using oxidation [P.A. Stolk et. al]

In this work, the process steps are tested with the TCAD simulations and presented optimized values for carrying the fabrication process using this tool. The paper is organized as Section II describes about the simulation process used, results obtained for various oxidation, diffusion and annealing techniques have been reported in section III. Finally, section IV summarizes with the conclusion.

II. Simulation environment

All the simulations have been carried out by the Synopsys TCAD simulator. It has been stated and proved that the TCAD is a sophisticated device level tool, which is suitable for modelling and characterizing as similar to that of practical IC fabrication processes. The simulation environment used in this work is Sentaurus process (Sprocess). The works that are carried out using this tool are reported in the Fig. 1, such as oxidation, diffusion and annealing mechanisms. As per the recent advances in diffusion mechanism such as ion-implantation, the work is carried out to show the optimized performance in these processing flows. Silicon is considered as the base material, with the dopants of boron (p-type) and phosphorus (n-type) materials have been considered in order to analyse the performance metrics.

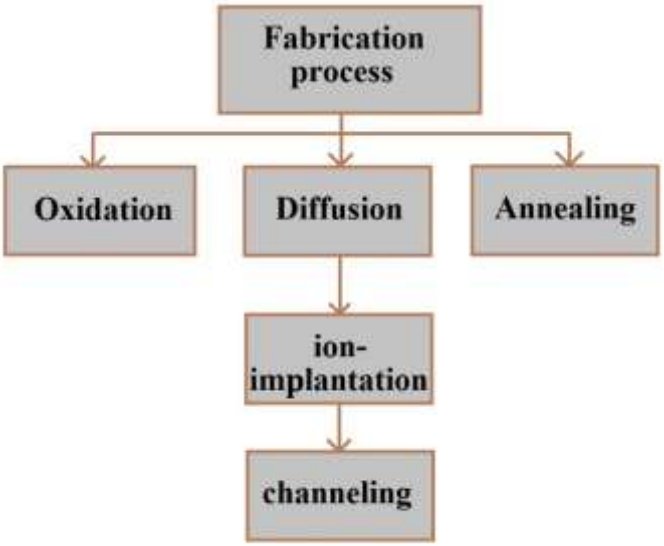

Fig. 1. Typical IC fabrication process used in this work.

III. Results and discussion

A. Oxidation:

It is defined as the process of growing oxide on to a substrate. Having many advantages of oxidation such as, masking element, surface passivation, gate oxide in MOS devices, and as isolation between devices, it has become an important processing step in the IC fabrication. The simulation test is carried out by taking a silicon sample and growing an oxide layer on top of the sample using thermal oxidation process [R.R. Razouk et. al]. The grown oxide on the silicon surface isotropically is shown in Fig. 2.

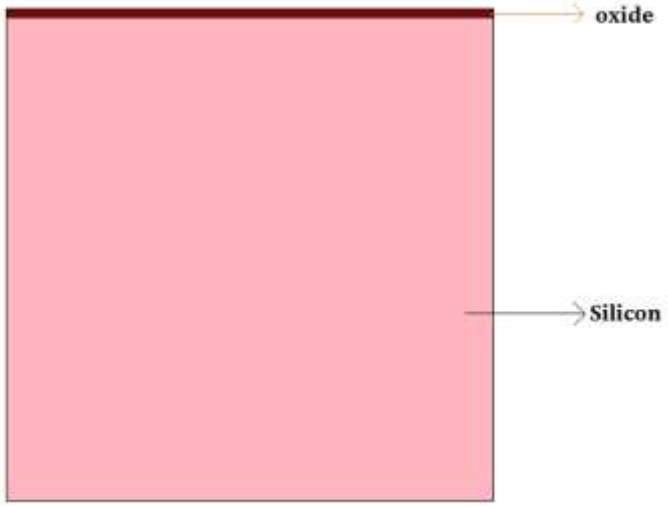

Fig. 2. Typical IC fabrication process used in this work.

The growth rate obtained at different timing slots by varying the temperature is depicted in Fig. 3.

This characteristics are well defined from the Deal Grove grow model for oxidation- kinetic Equation [R.R. Razouk et. al].

$$x^2 + Ax = B(t + \tau) \quad (1)$$

where $\tau = \frac{x_i^2 + Ax_i}{B}$ (2)

as 't' tends to zero then,

$$x = \frac{B(t + \tau)}{A} \quad (3)$$

as 't' tends to infinite then,

$$x = \sqrt{B(t + \tau)} \quad (4)$$

From the equations (3) & (4), it can be clear that the oxidation rate depends on two factors such as linear rate constant (B/A) and Parabolic constant (B).

It can be clear from the plot that, growth of oxidation can be taken place at the higher temperatures such as above 800°C. It can also be clear that for an increasing temperature the higher growth has been taken place in linear and parabolic manners (equations (3) & (4) are the evident).

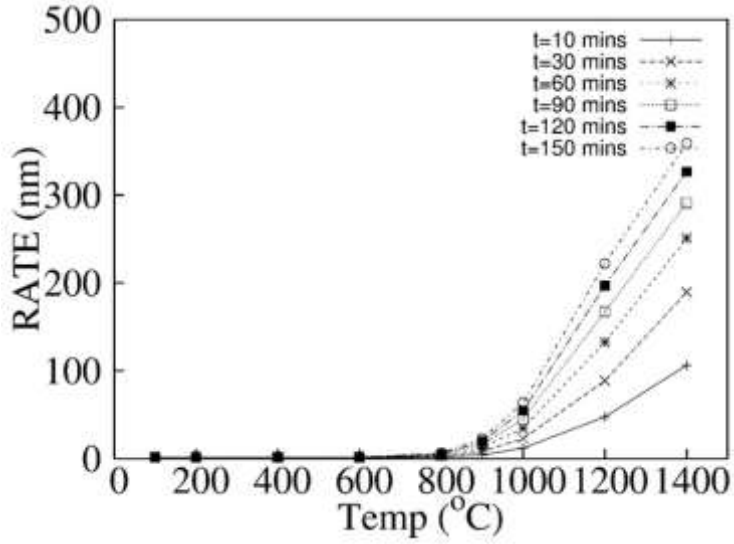

Fig. 3. Oxidation results at different timeslots for the variation of temperature using Sprocess in TCAD

The simulations are also having been performed for growth rate with respect to the processing time at constant temperature conditions for the identification of its optimized performance. The results are depicted in the Fig. 4. From these results, it is evident that the higher processing time lead to the higher growth rate, but the factor of achievement of oxidation growth rate in comparison with the higher temperature consideration is having less impact. Hence from these results, the optimized performance metrics for oxidation are higher temperature with moderate/low processing time.

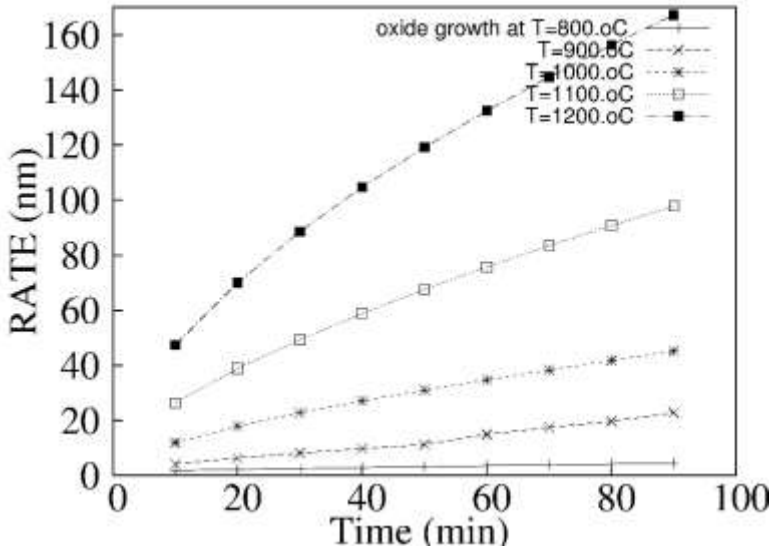

Fig. 4. Oxidation results at different temperatures for the variation of time (minutes) using Sprocess in TCAD

B. Diffusion

The process of movement of dopant atoms inside the crystal lattice is called as diffusion, which can be performed in three categories such as substitution, interstitial and interstitialcy. Ion-implantation is a more sophisticated process for diffusion, which obviously offers better control over the other diffusion processes. It is because of dependence of doping profile by the parameters such as dose and energy, which more convenient in the variation of dopant properties. Ion-implantation profile is defined by simply as Gaussian Function [I. Brodie et. al],

$$N(x) = NR_p \exp^{-\frac{(x-R_p)^2}{2\Delta R_p^{\,2}}} \quad (5)$$

Fig. 5 shows the total impurity doping concentration for various energy levels by keeping the dose as constant of $1\times e^{12}$. It can be seen from the plot that the increase in energy level will shift the doping concentration to the deeper of the crystal. Since the conduction mechanism in a device will only present at the surface of the crystal, the lower energy is preferred.

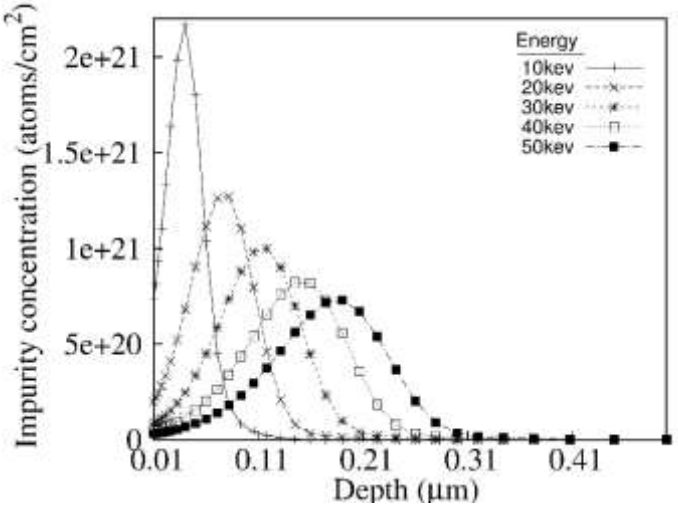

Fig. 5. Implantation profile for at constant dose with variation in energy using Sprocess in TCAD

Fig. 6 shows the total impurity concentration achieved for a variation in dose of in the ion-implantation process at a fixed energy of 10 keV. As it is observed that the increase in dose reflects the higher doping profile, but the higher doping profile yields to the too much miss alignments in the lattice structure, which can cause difficulty in overcoming through the annealing process. Hence an optimized value of dose is preferred in the range of $1\times e^{15}$ to $1\times e^{17}$ in order to reduce the miss-alignments occur during the implantation.

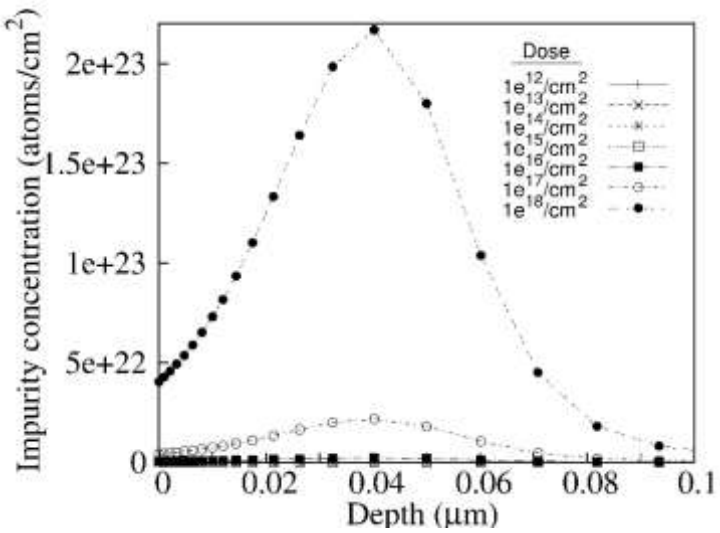

Fig. 6. Implantation profile for at constant energy with variation in dose using Sprocess in TCAD

Channelling:

An important parameter that plays as the key role in ion-implantation is the channelling mechanism. During the ion-implantation: while the beam is directed along a crystallographic axis, it is possible for the incident ion beams to find the corridor in between the lattice atoms in the interstitial space. And it is possible to find the empty passage way between the arrays of atoms through which the ions can be move forwarded to a considerable distance without any collision, this is the phenomena where the channelling might occur. This parameter has to be lower in order to avoid the loss of ions that are moving away from the lattice structure. Having many approaches in reducing the channelling, the most sophisticated technique is aligning the crystal with a sophisticated angle [S. Franssila et. al].

Fig. 7 shows the variation in doped impurity concentration for various angles of crystal orientation with respect to the ion beam. It can be clearly understood that the angle = 7^o shows the better Gaussian profile along the depth of the crystal. It is due to the dependence of crystal orientation for various semiconducting materials.

The critical crystalline distance has been given as [D.R. Myers et. al],

$$\rho_c = (\rho^2_{\min} + u^2_{rms})^{1/2} \quad (6)$$

Where lattice atoms displacement mentioned in rms value, ρ_{min} is the minimum atomic distance.

Here silicon crystal is taken as the base material for the doped n-type (Arsenic) impurities.

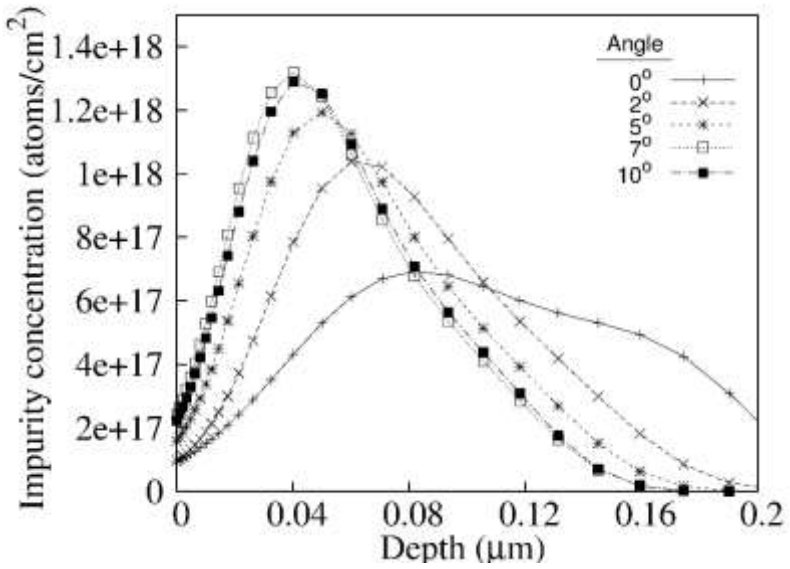

Fig. 7. Variation of tilting angle for reduction of channelling using Sprocess in TCAD

C. Annealing:

It is a process of realigning the misaligned crystal structure after the process of diffusion using ion-implantation.

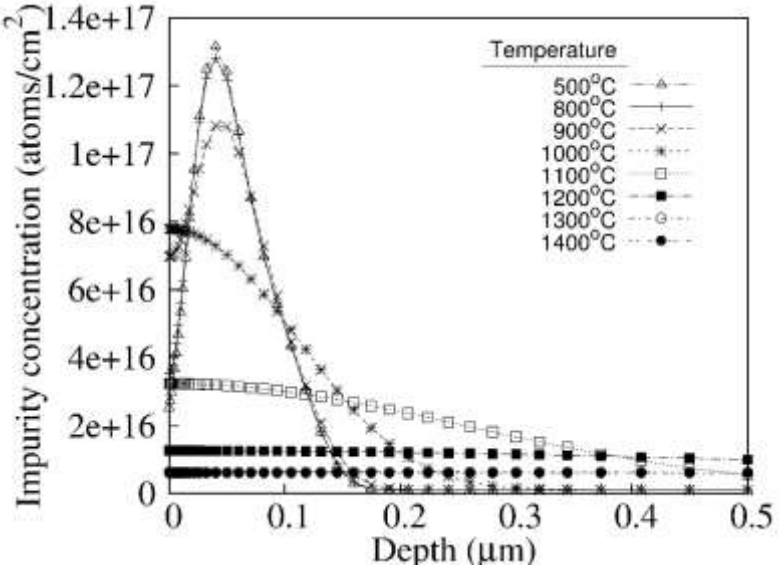

Fig. 8. Annealing at different temperature conditions for a misaligned crystal after the ion-implantation using Sprocess in TCAD

The Fig. 6 shows determination of temperature for reconstructing the misaligned structure of the crystal. It can be observed from the plot that, the impurity concentration is varied for a variable temperature. As the temperature increases the concentration at the surface initially increased and kept constant over the temperature range of above 1000°C. But in order to achieve a proper Gaussian profile as the concentration at the top surface should be high and the effective after the completion of ion implantation, this process can be termed as subjecting it to a drive-in. So, the doping profile may get considerably changed, while the D_t is considerably large. D_t may even become larger than the projected range but due to this the ion implantation profile may get

completely affected. So, these are the two major factors which will dictate your annealing time and temperature.

IV. CONCLUSION

In this work, the various results have been reported as the IC fabrication processing mechanisms. It has been concluded that the oxidation mechanism is well achieved with the high temperature and its moderate processing time. In the mechanism of diffusion process such as ion-implantation technique, the major results are shown and have been concluded that the higher energy and higher dose lead to higher penetration in to the wafer and more channelling. The channelling mechanism also tested and optimized result with the consideration of tilting angle of 7^{o} is finalized. Finally, the annealing technique and its metrics used to regain its crystal structure after the ion implantation mechanism have been included.

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